

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	6780	hot adj carrier	US-PGPUB; USPAT	OR	ON	2005/06/24 10:44
L2	16174	input adj pin	US-PGPUB; USPAT	OR	ON	2005/06/24 10:44
L3	19562	output adj pin	US-PGPUB; USPAT	OR	ON	2005/06/24 10:44
L4	38947	(delay adj time) and @ad<="19980706"	US-PGPUB; USPAT	OR	ON	2005/06/24 10:44
L5	450	transistor with connect\$ with (input adj pin)	US-PGPUB; USPAT	OR	ON	2005/06/24 10:44
L6	805	transistor with connect\$ with (output adj pin)	US-PGPUB; USPAT	OR	ON	2005/06/24 10:44
L7	0	(hot adj carrier) and ((delay adj time) and @ad<="19980706") and (transistor with connect\$ with (input adj pin)) and (transistor with connect\$ with (output adj pin))	US-PGPUB; USPAT	OR	ON	2005/06/24 10:44
L8	1	("5446676").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/24 10:44
L9	102	703/19.ccor.	US-PGPUB; USPAT	OR	ON	2005/06/24 10:44
L10	306	703/13.ccor.	US-PGPUB; USPAT	OR	ON	2005/06/24 10:44
L11	822	703/2.ccor.	US-PGPUB; USPAT	OR	ON	2005/06/24 10:44
L12	316	702/117.ccor.	US-PGPUB; USPAT	OR	ON	2005/06/24 10:44
L13	585	716/6.ccor.	US-PGPUB; USPAT	OR	ON	2005/06/24 10:44
L14	23	akimoto and hirata	JPO; DERWENT	OR	ON	2005/06/24 10:44
L15	22	(input adj slew) with calculat\$4	US-PGPUB; USPAT	OR	ON	2005/06/24 10:44
L16	3	(hot adj carrier) and (transistor with connect\$ with (input adj pin)) and (transistor with connect\$ with (output adj pin))	US-PGPUB; USPAT	OR	ON	2005/06/24 10:44
L17	10	((delay adj time) and @ad<="19980706") and (transistor with connect\$ with (input adj pin)) and (transistor with connect\$ with (output adj pin))	US-PGPUB; USPAT	OR	ON	2005/06/24 10:44

		Results
9.	(((pub-date > 1959 and pub-date < 1999 and FULL-TEXT(delay time) and FULL-TEXT(pin)) and stress) and transistor) and input) and output) and hot carrier [All Sources(- All Sciences -)]	2
8.	(((pub-date > 1959 and pub-date < 1999 and FULL-TEXT(delay time) and FULL-TEXT(pin)) and stress) and transistor) and input) and output [All Sources(- All Sciences -)]	16
7.	((pub-date > 1959 and pub-date < 1999 and FULL-TEXT(delay time) and FULL-TEXT(pin)) and stress) and transistor) and input [All Sources(- All Sciences -)]	19
6.	((pub-date > 1959 and pub-date < 1999 and FULL-TEXT(delay time) and FULL-TEXT(pin)) and stress) and transistor [All Sources(- All Sciences -)]	25
5.	(pub-date > 1959 and pub-date < 1999 and FULL-TEXT(delay time) and FULL-TEXT(pin)) and stress [All Sources(- All Sciences -)]	148
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3.	((pub-date > 1959 and pub-date < 1999 and FULL-TEXT(input pin) and FULL-TEXT(output pin)) and delay) and stress [All Sources(- All Sciences -)]	6
2.	(pub-date > 1959 and pub-date < 1999 and FULL-TEXT(input pin) and FULL-TEXT(output pin)) and delay [All Sources(- All Sciences -)]	55
1.	pub-date > 1959 and pub-date < 1999 and FULL-TEXT(input pin) and FULL-TEXT(output pin) [All Sources(- All Sciences -)]	122

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[Tamper Resistance - a Cautionary Note - Anderson, Kuhn \(1996\) \(Correct\) \(135 citations\)](#)

act like an RC element with a characteristic **time delay** the maximum usable clock frequency of a and check the personal identification numbers (**PINs**) with which customers authenticate themselves at and execution of individual instructions. Every **transistor** and its connection paths act like an RC element [www.cl.cam.ac.uk/users/cm213/Publications/tamper.ps.gz](http://www.cl.cam.ac.uk/users/cm213/Publications/tamper.ps.gz)

[A 5.26 Mflips Programmable Analogue Fuzzy Logic.. - Dualibe, Jespers.. \(2000\) \(Correct\)](#)

loser **transistors** M1. In this way the recovering **time delay** of these cells (i.e. when any of them pass from (Mega fuzzy logic inferences per second) at the **pin** terminals (CL=13pF) 933 W power consumption per whose shape is nearly an inverted trapezoid. **Transistors** ML2, MR2 have fixed large sizes, so that their [www.dice.ucl.ac.be/~verleyse/papers/iscas00cd.pdf](http://www.dice.ucl.ac.be/~verleyse/papers/iscas00cd.pdf)

[Backpropagation Hardware Based on Bit-Stream.. - Hein, Köllmann.. \(1996\) \(Correct\)](#)

(1 kW/m<sup>2</sup> Figure 6 shows the simulated **delay time** for a single On-chip resistor On-chip optical power level are in progress. Using external **pin**-photodiodes with discrete amplifiers instead of In a standard CMOS process a vertical bipolar **transistor** can be used as a photosensitive element. The [www.unibw-hamburg.de/EWEB/TI/postscript/1996/neurap\\_96.ps](http://www.unibw-hamburg.de/EWEB/TI/postscript/1996/neurap_96.ps)

[Analogue Optical Links for the CMS Tracker Readout System - Arbet-Engels, Cervelli, .. \(1997\) \(Correct\)](#)

gain 4 is calculated to be 1.14 W/mV. The **time delay** with the present transmitter configuration is fibres to the counting room and detected using **PIN** photodiodes. Results recently obtained with a a reference input resistor of a monolithic dual **transistor** current mirror. The modulation current is [www.cern.ch/CERN/Divisions/ECP/CME/OpticalLinks/wdocs/Elba1997Vincent.pdf](http://www.cern.ch/CERN/Divisions/ECP/CME/OpticalLinks/wdocs/Elba1997Vincent.pdf)

[A Power and Delay Optimization Method Using Input.. - Masanori Hashimoto.. \(1999\) \(Correct\)](#)

gate have an influence on the power dissipation **delay time**, and transition time of the CMOS gate. high switching probability (0.9) is needed with a **pin** which has small input capacitance. Here, a small 5.3% on average. key words: input reordering, **transistor** reordering, power estimation 1. Introduction [search.ieice.org/1999/files/...pdf/e82-a\\_1\\_159.pdf](http://search.ieice.org/1999/files/...pdf/e82-a_1_159.pdf)

[Combinatorial Aspects of Lower Power Clock Layout Synthesis in VLSI .. - Cho \(Correct\)](#)

skew must be less than 5% of the critical path **delay time** to build high performance system. Timing with length. Hence the use of buffers makes **time delay** linear with length by dividing the pulses must arrive nearly simultaneous at the clock **pins** of all clocked components. The difference in [vada.skku.ac.kr/Project/published/clock\\_lp.ps](http://vada.skku.ac.kr/Project/published/clock_lp.ps)

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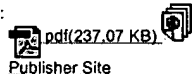
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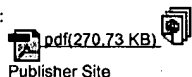

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